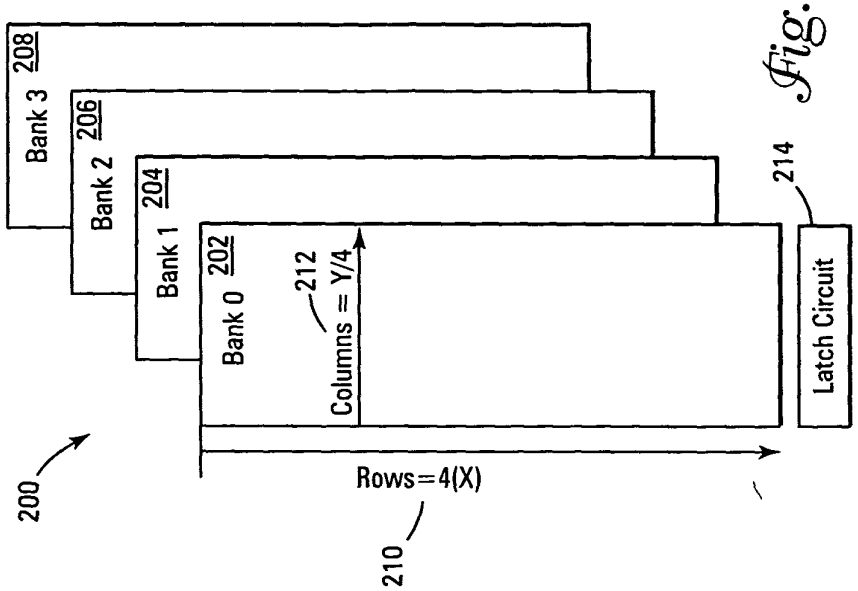


Fig. 2

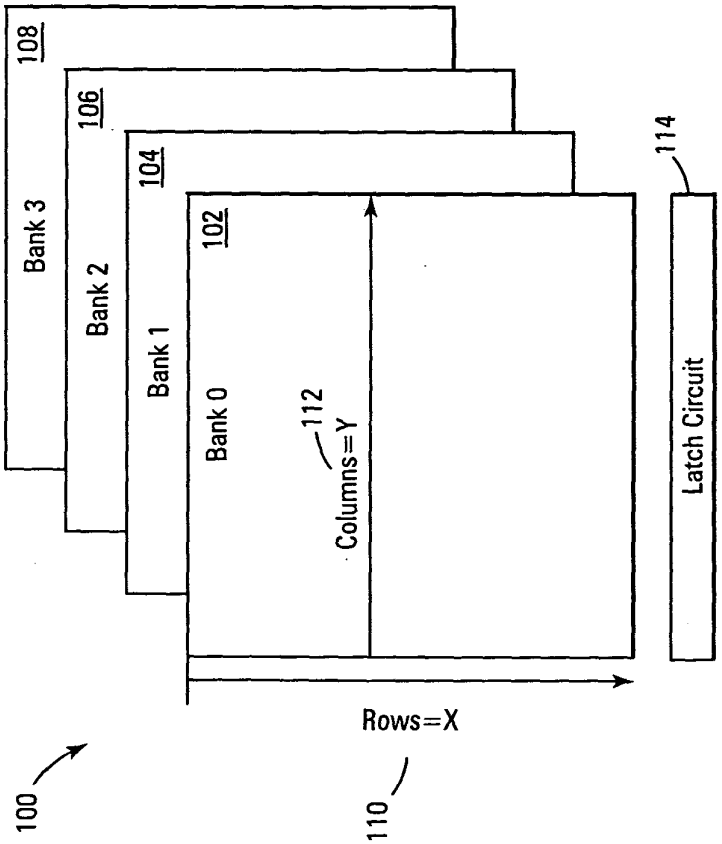


Fig. 1
Prior Art

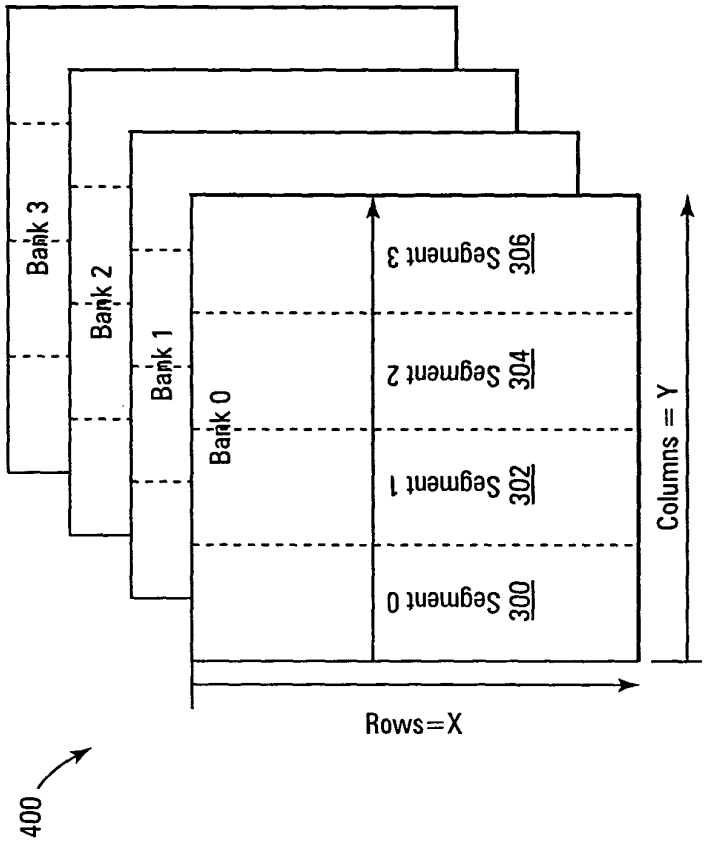
Bank 3
Bank 2
Bank 1
Bank 0
Segment 3 306
Segment 2 304
Segment 1 302
Segment 0 300
Columns = Y
Rows=X
400

Fig. 4

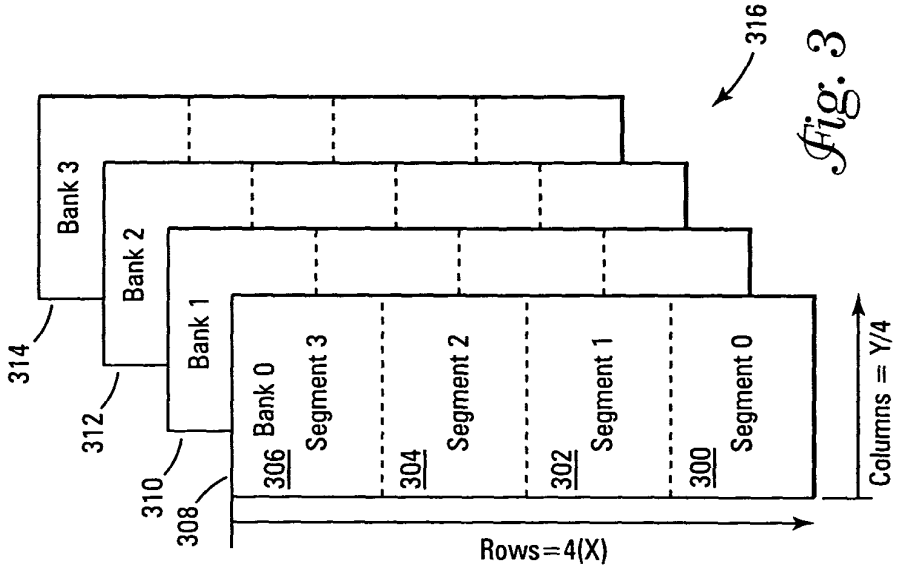
316
Bank 3
Bank 2
Bank 1
Bank 0
Segment 3
Segment 2
Segment 1
Segment 0
306
304
302
300
314
312
310
308
Columns = Y/4
Rows=4(X)

Fig. 3

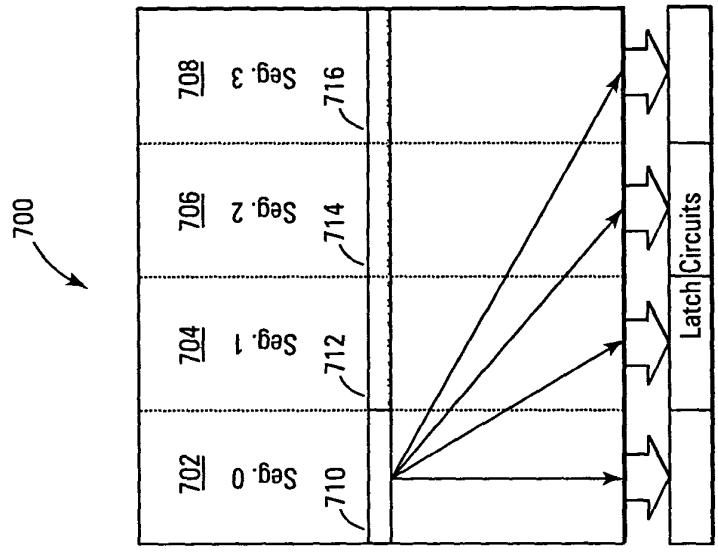
700
Seg. 0
Seg. 1
Seg. 2
Seg. 3
702
704
706
708
710
712
714
716
Latch Circuits

Fig. 7

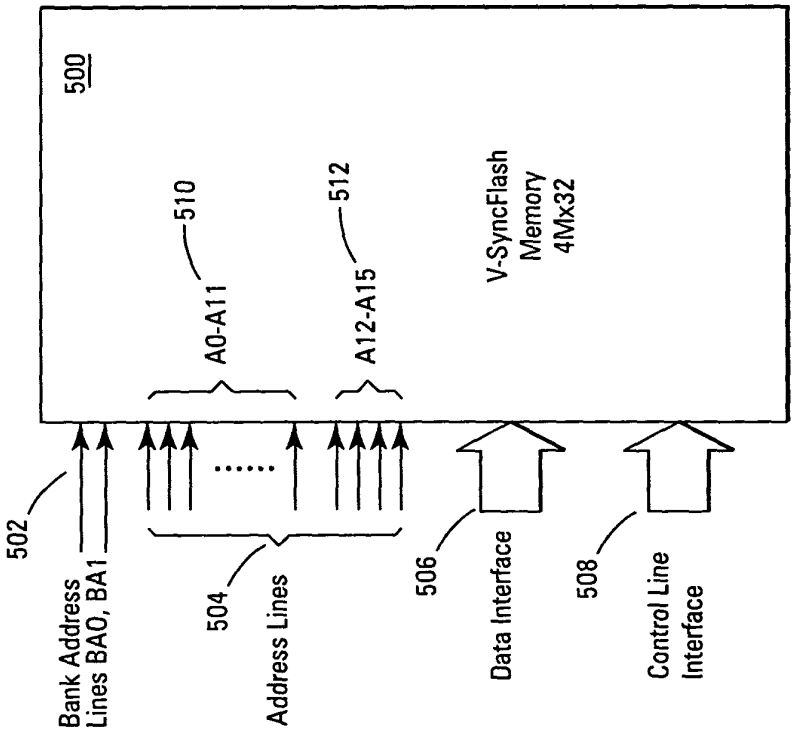
500
A0-A11
A12-A15
510
512
V-SyncFlash
Memory
4Mx32
502
Bank Address
Lines BA0, BA1
504
Address Lines
506
Data Interface
508
Control Line
Interface

Fig. 5

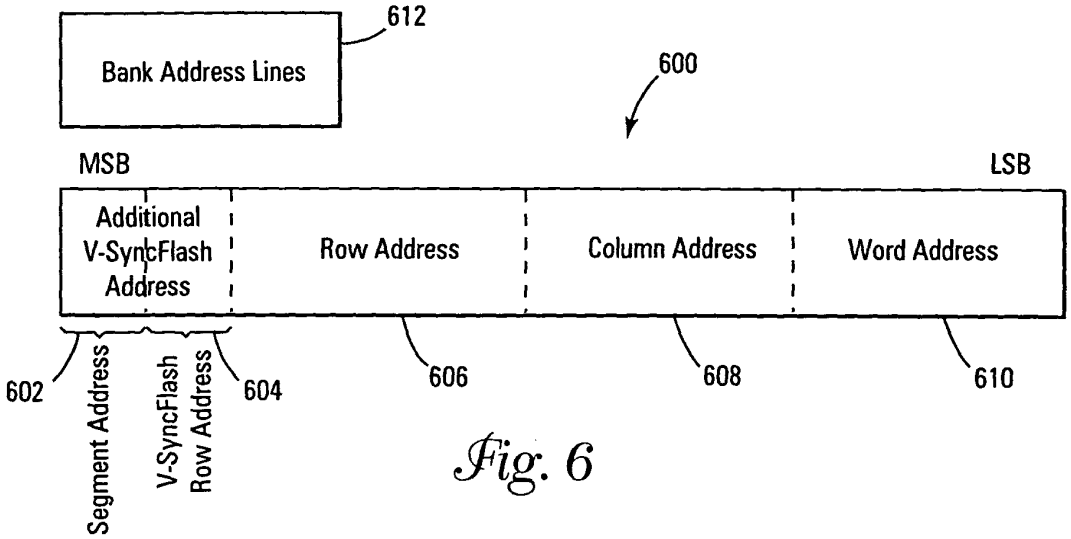
612
Bank Address Lines
600
MSB
LSB
Additional V-SyncFlash Address
Row Address
Column Address
Word Address
602
Segment Address
V-SyncFlash Row Address
604
606
608
610

*Fig. 6*

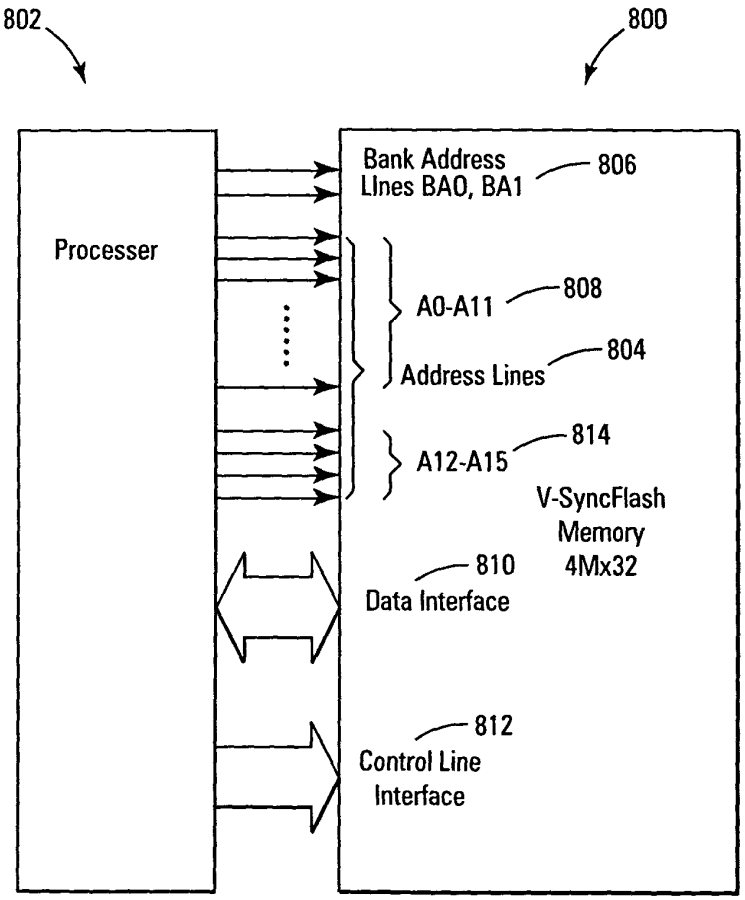
802
800
Processer
Bank Address Lines BA0, BA1
806
A0-A11
808
Address Lines
804
A12-A15
814
V-SyncFlash Memory 4Mx32
810
Data Interface
812
Control Line Interface

*Fig. 8*

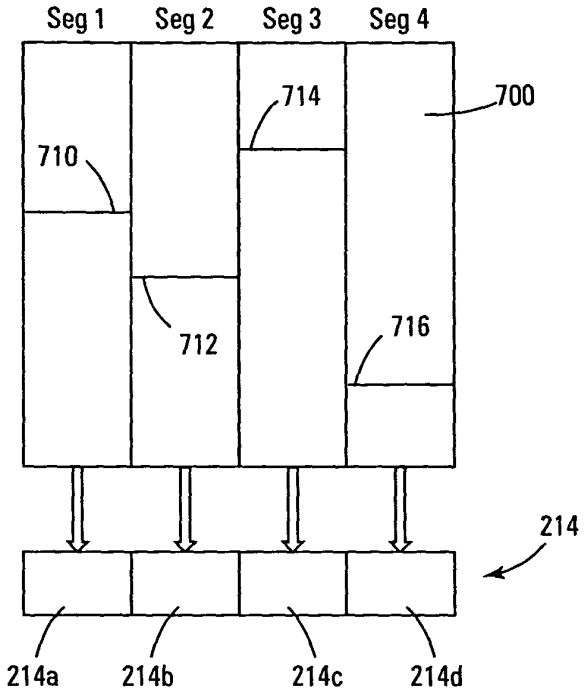
Seg 1
Seg 2
Seg 3
Seg 4
714
700
710
712
716
214
214a
214b
214c
214d

*Fig. 9*

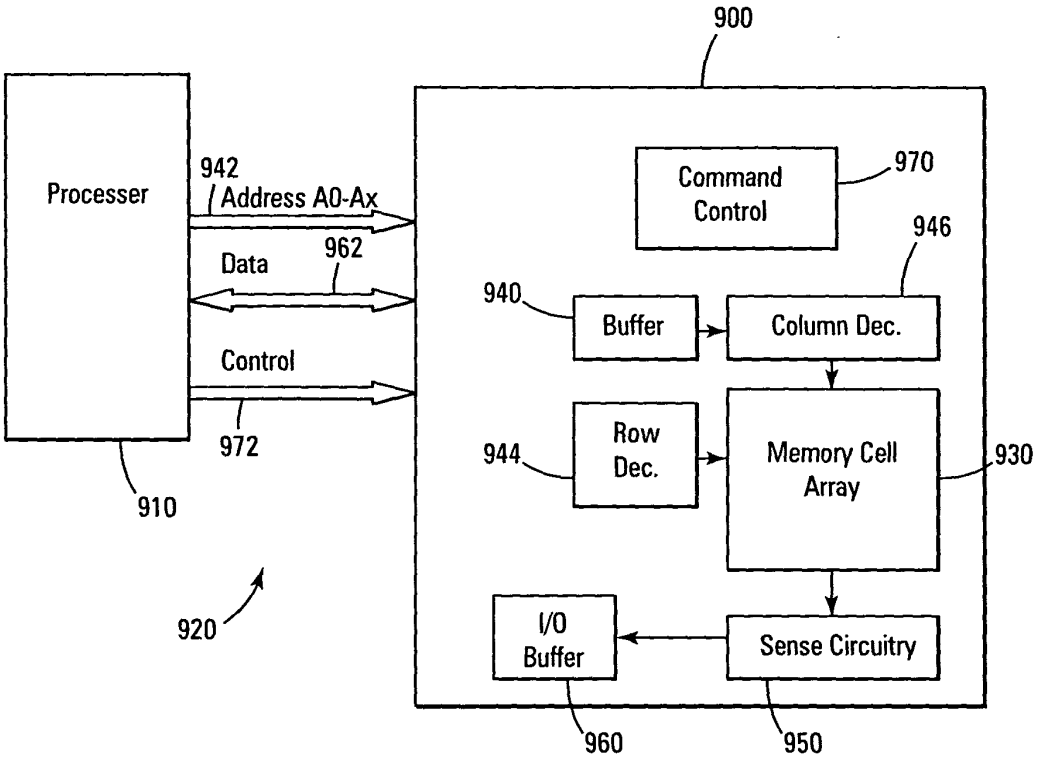
900
Processer
942
/ Address A0-Ax
Data
962
Control
972
910
920
Command Control
970
946
940
Buffer
Column Dec.
944
Row Dec.
Memory Cell Array
930
I/O Buffer
Sense Circuitry
960
950

*Fig. 10*

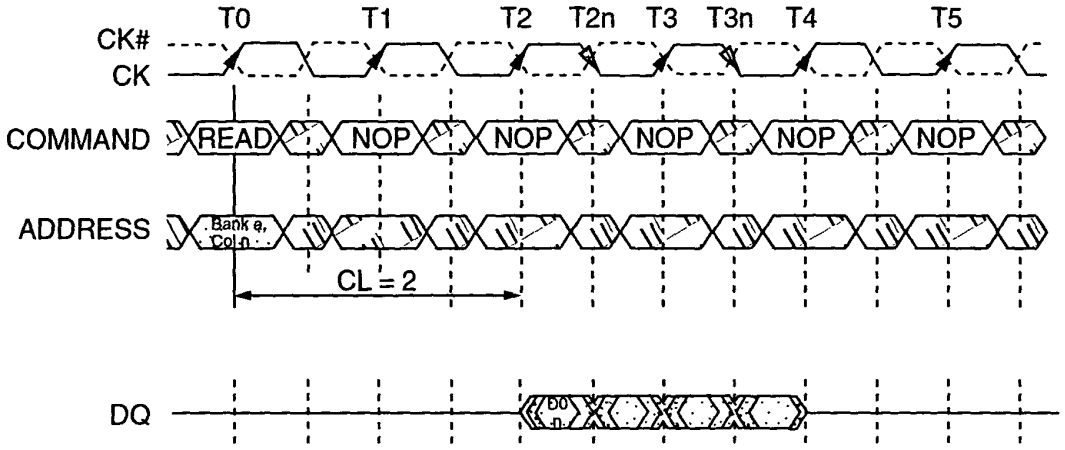
T0
T1
T2
T2n
T3
T3n
T4
T5
CK#
CK
COMMAND
READ
NOP
NOP
NOP
NOP
NOP
ADDRESS
Bank a, Col n
CL = 2
DQ
DO n

*Fig. 11*

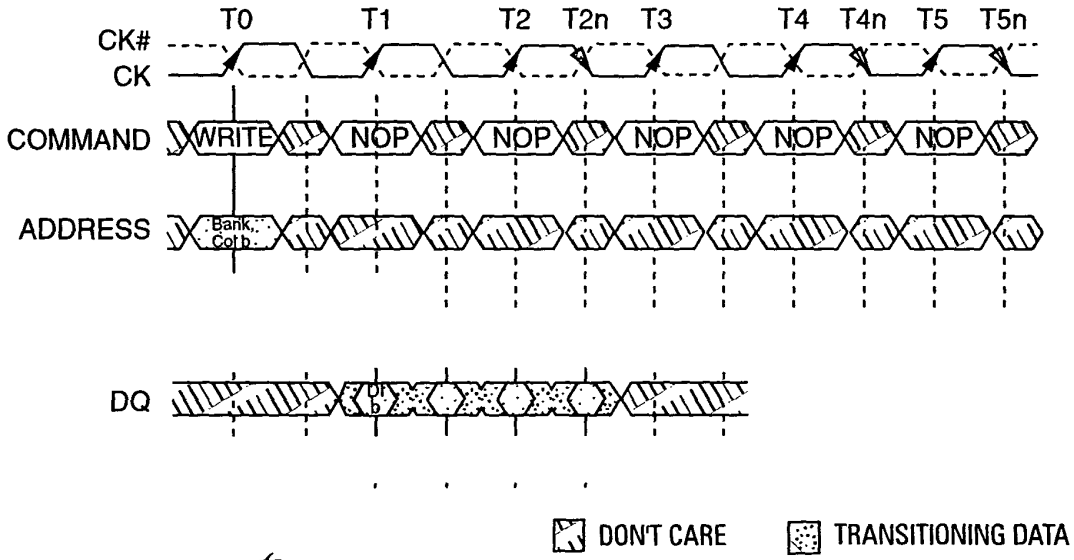
T0
T1
T2
T2n
T3
T4
T4n
T5
T5n
CK#
CK
COMMAND
WRITE
NOP
NOP
NOP
NOP
NOP
ADDRESS
Bank, Col b
DQ
DI b
DON'T CARE
TRANSITIONING DATA

*Fig. 12*